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PLANAR PEDESTAL MULTI-GATE DEVICE

Abstract

A method of forming a transistor comprises disposing a planar platform (or pedestal, or layer) of silicon atop a support structure of oxide which is atop a substrate; forming gate structures both atop and beneath the planar platform; and forming source and drain diffusions within the planar platform. The gate structures which are formed beneath the planar platform may smaller than the planar platform, and may be aligned with the gate structures which are formed atop the planar platform. A transistor formed by the method is also disclosed.